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EXAMINER

TURNER, ASHLEY D

ART UNIT	PAPER NUMBER
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2154

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/661,901	Applicant(s) KLOTZ ET AL.	
	Examiner ASHLEY D. TURNER	Art Unit 2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 January 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 and 17-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 and 17-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>1/30/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

The Examiner withdraws the claim objections of claims 2, 7,9,12,13,15,21 so Applicant's arguments are moot.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Sharon (US 6,205,122 B1) in view of Jayaraman (US 7,301,990 B2).

Referring to claim 1, Sharon discloses the limitations of a method for determining network topology (Abstract), comprising capturing and storing channelized data with a network analyzer (Col. 7 lines 63-66 Col. 8 lines 20-28); Sharon did not disclose interleaving the channelized data into a unitary data stream in chronological order; and processing the unitary data stream to extrapolate indicators of network element. The general concept of interleaving the channelized data into a unitary data stream in chronological order; and processing the unitary data stream to extrapolate indicators of network element is well known in the art as taught by Jayaraman.

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Jayaraman discloses interleaving the channelized data into a unitary data stream in chronological order; and processing the unitary data stream to extrapolate indicators of network element. (FIG. 2 shows a block diagram of a base station 110i (which is one of the base stations shown in FIG. 1) and terminal 120. On the forward link, at base station 101i, data to be transmitted on the forward link to the terminals and for overhead channels is provided from a data source 212 to a transmit (TX) data processor 214. TX data processor 214 formats, codes, interleaves and modulates the data for each terminal and each overhead channel to provide data modulation symbols (or simply, data symbols) for that terminal/channel. A TX channel processor 216 then receives and channelizes the data symbols and pilot symbols onto different code channels. TX channel processor 216 further combines and spectrally spreads the channelized data and pilot symbols with a complex pseudo-random number (PN) sequence assigned to base station 110i to provide a stream of transmit chips (denoted as $[x_{\text{sub.k.sup.i}}]$). The processing by processors 214 and 216 is described in further detail below. A transmitter unit (TMTR) 218 then converts the stream of transmit chips into one or more analog signals, and further conditions (e.g., amplifies, filters, and frequency upconverts) the analog signals to generate a modulated signal. The modulated signal is then transmitted via an antenna 220 and over a wireless channel). It would have been obvious to one of ordinary skill in the art at the time of to modify Sharon to include interleaving the channelized data into a unitary data stream in chronological order; and processing the unitary data stream to extrapolate indicators of network element in order to determine the entire network topology.

Claims 2, 16 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Sharon (US 6,205,122 B1) in view of Jayaraman (US 7,301,990 B2) further in view of Ikeda (US 2003/0063571 A1).

Referring to claim 2, Sharon and Jayaraman discloses all the limitations of claim 2 which are described above. Sharon did not disclose the limitation of processing the unitary data stream further comprises determining a left and right topology from the network analyzer. The general concept of processing the unitary data stream further comprises determining a left and right topology from the network analyzer is well known in the art as taught by Ikeda. Ikeda discloses processing the unitary data stream further comprises determining a left and right topology from the network analyzer (Abstract). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sharon to include processing the unitary data stream further comprises determining a left and right topology from the network analyzer in order to determine the entire network topology.

Referring to claim 16 Sharon and Jayaraman discloses all the limitations of claim 16 which is described above. Sharon did not disclose combining the left and right channel data into a unitary data stream. The general concept of combining the left and right channel data into a unitary data stream is well known in the art as taught by Ikeda. Ikeda discloses combining the left and right channel data into a unitary data stream (Abstract). It would have been obvious to one of ordinary

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skill in the art at the time of the invention to modify Sharon to include combining the left and right channel data into a unitary data stream in order to determine the entire network topology.

Claims 3-6 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Sharon (US 6,205,122 B1) in view of Jayaraman (US 7,301,990 B2) further in view of Ikeda (US 2003/0063571 A1) further in view of Warren (US 2004/0081186 A1).

Referring to claim 3, Sharon, Ikeda and Ikeda disclose all the limitations of claim 3 which is described above. Ikeda also discloses ordering of events in the unitary data stream to determine the presence of network elements [0031]. Ikeda did not disclose analyzing ordered sets, source and destination Ids. The general concept of analyzing ordered sets, source and destination Ids is well known in the art as taught by Warren. Warren discloses analyzing ordered sets, source and destination Ids [0240], [0161]. It would have been obvious to one of ordinary skill in the art to modify Sharon to include analyzing ordered sets, source and destination Ids in order to monitor the data going through the network.

Referring to claim 4, Sharon, Jayaraman, Ikeda, and Warren discloses all the limitations of claim 4 which is described above. Sharon and Ikeda did not disclose analyzing open and close commands in the unitary data stream to determine the presence of a loop. The general concept of analyzing open and close commands in the unitary data trace to determine the presence of a loop

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is well known in the art as taught by Warren. Warren discloses analyzing open and close commands in the unitary data trace to determine the presence of a loop (Warren; [0015]). It would be obvious to one of ordinary skill in the art at the time of the invention to modify Sharon to include analyzing open and close commands in the unitary data trace to determine the presence of a loop in order to send and receive data back to the terminal.

Referring to claim 5 Sharon, Jayaraman, Ikeda, and Warren discloses all the limitations of claim 5 which is described above. Sharon did not disclose analyzing device addresses in the unitary data trace to determine the presence of switches. The general concept of analyzing device addresses in the unitary data trace to determine the presence of switches is well known in the art as taught by Warren. Warren discloses analyzing device addresses in the unitary data trace to determine the presence of switches [0592]. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sharon invention to include analyzing device addresses in the unitary data trace to determine the presence of switches in order to provide a device that has control of the loop.

Referring to claim 6 Sharon, Jayaraman, Ikeda, and Warren discloses all the limitations of claim 6 which is described above. Sharon did not disclose analyzing the ordering of events in the unitary data trace to determine the presence of stealth mode switches. The general concept of analyzing ordering of events in the unitary data stream to determine the presence of stealth mode switches is well known as taught by Warren. Warren discloses analyzing ordering of events in

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the unitary data trace to determine the presence of stealth mode switches [0411]. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sharon to include analyzing ordering of events in the unitary data trace to determine the presence of stealth mode switches in order to provide a device that has control of the loop.

Claim 7 is rejected under 35 U.S.C. 103 (a) as being unpatentable Ikeda (US 2003/0063571 A1) in view of Warren (US 2004/0081186 A1).

Referring to claim 7 Ikeda disclose a method for determining network topology during a network analysis process, positioning a plurality of network analyzers in communication with the network (Abstract); capturing trace data from a first and second channel on each of the analyzers (Abstract); determining a first topology corresponding to the first channel of each said analyzer (Fig 21 A); determining a second topology corresponding to the second channel of each said analyzer (Fig .21 A and Fig 21 B.), combining the first and second topologies from each of the analyzers(Fig. 21 A [0155]. Ikeda did not disclose deleting duplicate topology entries from the combined topology to generate the network topology. The general concept of deleting duplicate topology entries from the combined topology to generate the network topology is well known in the art as taught by Pulsipher. Pulsipher discloses deleting duplicate topology entries from the combined topology to generate the network topology (Col. 10 lines 55-65 and Col. 11 lines 1-6). It would have been obvious to one of ordinary skill in the art at the time of the invention to

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modify Ikeda to include deleting duplicate topology entries from the combined topology to generate the network topology in order to derive a global view of the network.

Referring to claim 9, Warren discloses all the limitations of claim 9 which is described above.

Warren did not disclose the capturing the trace data further comprising storing channelized data for subsequent processing. The general concept of the capturing the trace data further comprising storing channelized data for subsequent processing is well known in the art as taught by Sharon.

Sharon discloses the capturing the trace data further comprising storing channelized data for subsequent processing. (Col. 7 lines 63-66 Col. 8 lines 20-28). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Warren to include the capturing the trace data further comprising storing channelized data for subsequent processing in order to derive a global view of the network.

Referring to claim 10 Ikeda and Warren discloses all the limitation of claim 8 which are described above. Ikeda did not disclose determining the first and second topology analyzing ordered sets, source and destination identifications, device addresses, and ordering of events in the trace data to determine the presence of network elements that correspond to the ordered sets, source and destination identifications, and device addresses. The general concept of determining the first and second topology analyzing ordered sets, source and destination identifications, device addresses, and ordering of events in the trace data to determine the presence of network

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elements that correspond to the ordered sets, source and destination identifications, and device addresses is well known in the art as taught by Warren. Warren discloses determining the first and second topology analyzing ordered sets, source and destination identifications, device addresses, and ordering of events in the trace data to determine the presence of network elements that correspond to the ordered sets, source and destination identifications, and device addresses (Abstract). [0160], [0161], [0202]. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ikeda to include determining the first and second topology analyzing ordered sets, source and destination identifications, device addresses, and ordering of events in the trace data to determine the presence of network elements that correspond to the ordered sets, source and destination identifications, and device addresses in order to monitor the data going through the network.

Referring to claim 11, Ikeda and Warren disclose all the limitations of claim 11 which is described above. Ikeda did not disclose analyzing open and close commands in the unitary data trace to determine the presence of a loop. The general concept of analyzing open and close commands in the unitary data trace to determine the presence of a loop is well known in the art as taught by Warren. Warren discloses analyzing open and close commands in the unitary data trace to determine the presence of a loop (Warren; [0015]). It would be obvious to one of ordinary skill in the art at the time of the invention to modify Ikeda to include analyzing open and close commands in the unitary data trace to determine the presence of a loop in order to send and receive data back to the terminal.

Referring to claim 12 Ikeda and Warren discloses all the limitations of claim 12 which is described above. Ikeda did not disclose analyzing the device addresses in the unitary data trace to determine the presence of switches. The general concept of analyzing device addresses in the unitary data trace to determine the presence of switches is well known in the art as taught by Warren. Warren discloses analyzing the device addresses in the unitary data trace to determine the presence of switches (Warren; [0592]). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ikeda invention to include analyzing device addresses in the unitary data trace to determine the presence of switches in order to provide a device that has control of the loop.

Referring to claim 13 Ikeda and Warren discloses all the limitations of claim 13 which is described above. Ikeda did not disclose analyzing the ordering of events in the unitary data trace to determine the presence of stealth mode switches. The general concept of analyzing ordering of events in the unitary data trace to determine the presence of stealth mode switches is well known as taught by Warren. Warren discloses analyzing the ordering of events in the unitary data trace to determine the presence of stealth mode switches (Warren; [0411]). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ikeda to include analyzing the ordering of events in the unitary data trace to determine the presence of stealth mode switches in order to provide a device that has control of the loop.

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Claim 14 is rejected under 35 U.S.C. 103 (a) as being unpatentable Ikeda (US 2003/0063571 A1) in view of Warren (US 2004/0081186 A1) further in view of Pulsipher (5,948,055).

Referring to claim 14, Ikeda and Warren disclose all the limitations of claim 14 which is described above. Ikeda did not disclose displaying the network topology to a user via a graphical user interface. The general concept of displaying the network topology to a user via a graphical user interface is well known in the art as taught by Pulsipher. Pulsipher discloses displaying the network topology to a user via a graphical user interface (Abstract). It would have been obvious to one of ordinary skill in the art to modify Ikeda to include displaying the network topology to a user via a graphical user interface in order to display the results of the topology the user requested.

Claim 15 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Sharon (US 6,205,122 B1) in view of Smorgrav (US 6,615,261) B1.

Referring to claim 15 Sharon discloses analyzing a network to determine the topology of the network (Abstract), positioning at least one analyzer in communication with the network; capturing a left channel and a right channel data trace from each of the at least one analyzers; (Abstract); extrapolating network device presence indicators from the unitary data stream (Abstract); and determining the network topology from the network device presence indicators (Abstract) and displaying the determined network topology to a user (Col. 6 lines 59-67 System 10 also preferably features at least one, and preferably a plurality of, graphical user interfaces 16

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for interaction between the user and CME 12. Graphical user interface 16 displays the completed physical topology map to the user, as well as accepting instructions from the user to send to CME 12. Even without graphical user interface 16, however, the information about the physical topology map could still be displayed to the user through other display mechanisms.) . Sharon did not disclose combining the left and right channel data traces into a unitary data stream. The general concept of combining the left and right channel data traces into a unitary data stream is well known in the art as taught by Smorgrav. Smorgrav discloses combining the left and right channel data traces into a unitary data stream (Col. 6 lines 21-28 The input to the process is one or more streams of samples for a time interval; one stream for each data object collected from a network element, in chronological order. Each stream is then processed by the presentation layer which output is the same streams as the input, but where the streamed data are rearranged so that each stream has a one datapoint for the specific times, at a specific frequency, still in chronological order, as illustrated in FIG. 8.) It would have been obvious to one of ordinary skill in the art to modify Sharon to include combining the left and right channel data traces into a unitary data stream in order to display the results of the topology the user requested.

Claim 8 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Ikeda (US 2003/0063571 A1) in view of Sharon (US 6,205,122 B1).

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Referring to 8, Ikeda discloses all the limitations of claim 8 which are described above.

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Ikeda did not disclose wherein positioning the at least one network analyzer positioning the analyzers such that bi-directional communication between each network element may be captured in a data trace. The general concept of positioning the at least one network analyzer positioning the analyzers such that bi-directional communication between each network element may be captured in a data trace is well known in the art as taught by Sharon. Sharon discloses positioning the at least one-network analyzer positioning the analyzers such that bi-directional communication between each network element may be captured in a data trace (Abstract).

Claim 18 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Sharon (US 6,205,122 B1) further in view of Smorgrav (US 6,615,261) B1 further in view of Warren (US 2004/0081186 A1).

Referring to claim 18 Sharon and Smorgrav disclose all the limitation of claim 18 which are described above. Sharon did not disclose determining the first and second topology analyzing ordered sets, source and destination identifications, device addresses, and ordering of events in the trace data to determine the presence of network elements that correspond to the ordered sets, source and destination identifications, and device addresses. The general concept of determining the first and second topology analyzing ordered sets, source and destination identifications, device addresses, and ordering of events in the trace data to determine the presence of network elements that correspond to the ordered sets, source and destination identifications, and device

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addresses is well known in the art as taught by Warren. Warren discloses determining the first and second topology analyzing ordered sets, source and destination identifications, device addresses, and ordering of events in the trace data to determine the presence of network elements that correspond to the ordered sets, source and destination identifications, and device addresses (Abstract). [0160], [0161], [0202]. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ikeda to include determining the first and second topology analyzing ordered sets, source and destination identifications, device addresses, and ordering of events in the trace data to determine the presence of network elements that correspond to the ordered sets, source and destination identifications, and device addresses in order to monitor the data going through the network.

Referring to claim 19, Sharon and Smorgrav disclose all the limitations of claim 19 which is described above. Sharon did not disclose the ordered sets are analyzed to determine the presence of a loop on the network. The general concept of analyzing open and close commands in the unitary data trace to determine the presence of a loop is well known in the art as taught by Warren. Warren discloses the ordered sets are analyzed to determine the presence of a loop on the network [0015]. It would be obvious to one of ordinary skill in the art at the time of the invention to modify Sharon to include the ordered sets are analyzed to determine the presence of a loop on the network in order to send and receive data back to the terminal.

Referring to claim 20 Sharon, and Smorgrav discloses all the limitations of claim 20 which is described above. Sharon did not disclose the device addresses are analyzed to determine the

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presence of switches on the network. The general concept of the device addresses are analyzed to determine the presence of switches on the network is well known in the art as taught by Warren. Warren discloses analyzing device addresses in the unitary data trace to determine the presence of switches [0592]. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sharon invention to include the device addresses are analyzed to determine the presence of switches on the network in order to provide a device that has control of the loop.

Referring to claim 21 Sharon and Smorgrav discloses all the limitations of claim 21 which is described above. Sharon did not disclose the ordering of events is analyzed to determine the presence of stealth mode switches on the network. The general concept of the ordering of events is analyzed to determine the presence of stealth mode switches on the network is well known as taught by Warren. Warren discloses analyzing the ordering of events in the unitary data trace to determine the presence of stealth mode switches [0411]. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sharon to include the ordering of events is analyzed to determine the presence of stealth mode switches on the network in order to provide a device that has control of the loop.

Response to Arguments

Applicant's arguments filed on 1/11/2008 have been fully considered but they are deemed moot in view of the new grounds of rejections.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ashley D. Turner whose telephone number is 571-270-1603. The examiner can normally be reached on Monday thru Friday 7:30a.m.- 5:00p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ashley D Turner
Examiner
Art Unit 2154

/Nathan J. Flynn/

Supervisory Patent Examiner, Art Unit 2154